Http//:www.sh-willsemi.com

WD3151

3-Channel LED Driver

Descriptions

The WD3151 is a 3-channel LED driver designed to produce variety of lighting effects. The device has a program memory for creating variety of lighting sequences. When the program memory has been loaded, the WD3151 can operate independently without processor control.

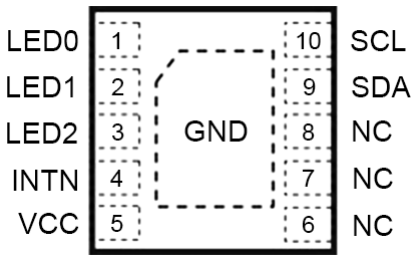
Three independent LED channels have accurate programmable current sinks, from 0mA to 15mA with 5mA steps and 8-bit flexible PWM control. Each channel can be configured into each of the three program execution engines. Program execution engines have program memory for creating desired lighting sequences with PWM control.

Features

- Supply voltage: 2.7V to 5.5V
- Three independently programmable LED outputs with 8-bit PWM control and 2-bit current setting (from 0mA to 15mA)
- Autonomous operation with three program execution engines
- Direct I^2C register control for lighting
- I^2C Compatible Interface
  - Power supply support 1.8V to 3.3V
  - Data transfers up to 400kbps
- INTN interrupt function
- Typical LED output saturation voltage 100mV and current matching ±1%
- Built-in oscillator with ±5% accuracy
- Low power consumption
  - Operating current: 100uA
  - Standby current: 20uA
- Operating temperature: -40℃ to 85℃
- ESD HBM 4kV
- DFN2*2-10L package

Applications

- Smart Phones
- Tablets
- Portable games



Pin configuration (Top view)

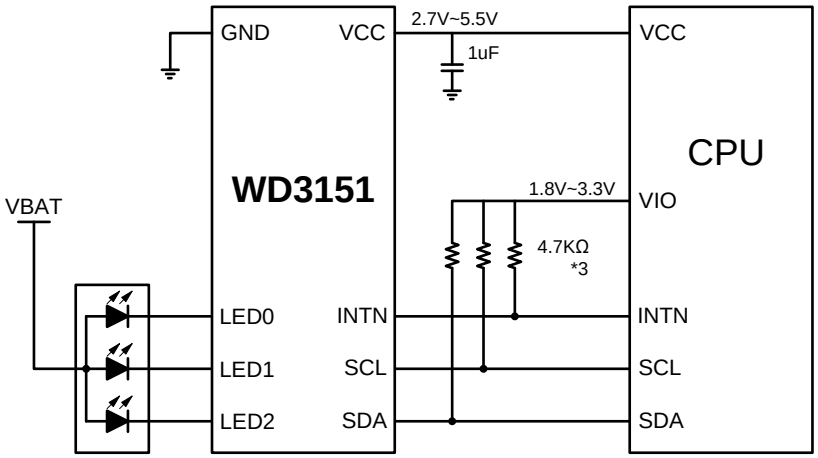
DFN2*2-10L

3151 = Device code
Y = Year code
W = Week code
Marking

Order information

Device	Package	Shipping
WD3151D-10/TR	DFN2*2-10L	3000/Reel&Tape

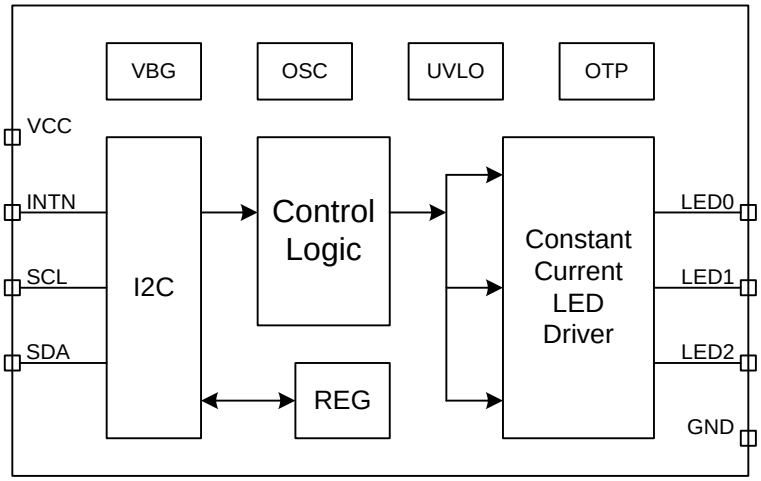
Typical applications



Pin descriptions

No.	Name	I/O	Description
1	LED0	Analog	LED driver current sink terminal
2	LED1	Analog	LED driver current sink terminal
3	LED2	Analog	LED driver current sink terminal
4	INTN	Open drain	Interrupt output
5	VCC	Power	2.7V~5.5V power supply
6	NC		Not internally connected
7	NC		Not internally connected
8	NC		Not internally connected
9	SDA	I/O	I^2C serial interface data input/output. 1.8V/3.3V compatible
10	SCL	I	I^2C serial interface clock. 1.8V/3.3V compatible
Power PAD	GND	Ground	Connect to ground.

Block diagram



Absolute maximum ratings *(1)*

Parameter	MIN	MAX	Unit
Power supply VCC	-0.3	6.0	V
Analog pins (LED0, LED1, LED2)	-0.3	6.0	V
Digital pins (SDA, SCL, INTN)	-0.3	VCC+0.3V with 6.0 max	V
Storage temperature T_{stg}	-65	150	℃
Junction temperature T_{JMAX}		150	℃
Maximum lead temperature		260	℃
Junction-to-ambient thermal resistance (DFN10L)	45		℃/W
ESD HBM	-4	4	kV
Latch-up	-450	450	mA

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	MIN	MAX	Unit
Power supply VCC	2.7	5.5	V
Digital pins	1.8	VCC	V
Junction temperature T_J	-40	125	℃
Ambient temperature T_A	-40	85	℃

Electronics Characteristics

Unless otherwise specified: limits for typical values are for T_A = 25℃ and minimum and maximum limits apply over the operating ambient temperature range (-40℃ < T_A < 85℃); VCC=3.6V and range (2.7V < VCC < 5.5V).

Symbol	Description	Test Conditions	MIN	TYP	MAX	Unit
I_{PS}	Standby current	Power on or command reset		20		uA
I_{CC}	Operating current	Register GCR=01h		100		uA
F_{OSC}	Oscillator frequency	Internal	227	252	278	kHz
LED driver (LED0, LED1, LED2) electrical characteristics (GCR=01h, PWM0~2=FFh)						
I_{MAX}	Maximum sink current	LCFG0~2=03h	14.55	15	15.45	mA
		LCFG0~2=02h	9.7	10	10.3	
		LCFG0~2=01h	4.85	5	5.15	
		LCFG0~2=00h		0		
I_{OUT}	Accuracy of output current *(2)*	LCFG0~2=03h		±2	±3	%
I_{match}	Matching *(2)*	LCFG0~2=03h		±1	±2	%
V_{SAT}	Saturation voltage *(3)*	LCFG0~2=03h		100		mV
F_{LED}	PWM switching frequency			250		Hz

(2) Output current accuracy is the difference between the actual value of the output current and programmed value of this current. Matching is the maximum difference from the average. For the constant current outputs on the part, the following are determined: the maximum output current (MAX), the minimum output current (MIN), and the average output current of all outputs (AVG). Two matching numbers are calculated: (MAX - AVG)/AVG and (AVG - MIN)/AVG. The largest number of the two (worst case) is considered the matching figure. Note that some manufacturers have different definitions in use.

(3) Saturation voltage is defined as the voltage when the LED current has dropped 10% from the set value.

Logic interface characteristics

Unless otherwise specified: limits for typical values are for TA = 25℃ and minimum and maximum limits apply over the operating ambient temperature range (-40℃ < TA < 85℃); VCC=3.6V and range (2.7V < VCC < 5.5V).

Symbol	Description	MIN	TYP	MAX	Unit
Logic input SCL and SDA characteristics					
V_{IH}	Input high level	1.2			V
V_{IL}	Input low level			0.6	V
I_{IH}	High level input current		5		nA
I_{IL}	Low level input current		5		nA
Logic output SDA characteristics					
V_{OL}	Output low level (I_{OUT} = 3mA)		0.3	0.5	V
I_L	Output leakage current			1	uA
I^2C timing requirements *(4)*					
F_{SCL}	I^2C clock frequency			400	kHz
t_{BUF}	Bus-free time between a STOP and a START condition	1.3			uS
$t_{HD,STA}$	Hold time (repeated) START condition	0.6			uS
t_{LOW}	Clock low time	1.3			uS
t_{HIGH}	Clock high time	0.6			uS
$t_{SU,STA}$	Setup time for a repeated START condition	1.3			uS
$t_{HD,DAT}$	Data hold time	0.05			uS
$t_{SU,DAT}$	Data setup time	0.1			uS
t_R	Rise time of SCL			0.3	uS
t_F	Fall time of SCL			0.3	uS
$t_{SU,STO}$	Set-up time for STOP condition	0.6			uS
T_{SP}	SCL input deglitch			200	nS
	SDA input deglitch			250	nS
C_b	Capacitive load for each bus line			400	pF

(4) Specification is ensured by design and is not tested in production.

Fig4 is the timing parameters of I^2C interface (SCL, SDA).

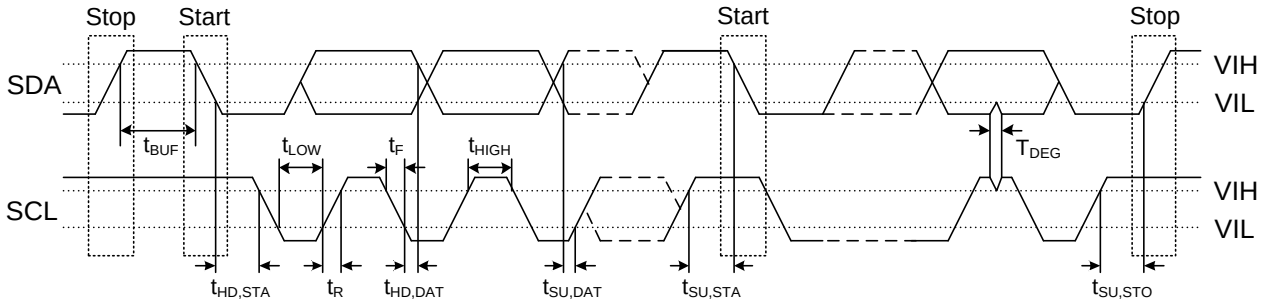


Fig4 I^2C timing parameters

Operation Mode

Reset

In the reset mode all the internal registers are reset to the default values and the chip will enter the standby mode.

Reset is down always if “55h” is written to Reset Register or internal Power On Reset (POR) is activated. POR will activate when supply voltage VCC rises above 2.3V (typical). Once VCC falls below 2.15V (typical), POR will inactivate. PUIS control bit is high after POR by default.

Standby Mode

The standby mode is entered if POR is activated. This is the low power consumption mode, when the needed internal blocks (VBG, UVLO, OTP etc.) are enabled, and the power consumption is lower than 20uA.

Operating Mode

If LEDE bit (GCR Register) is set to 1, the chip will enter operating mode.
In the operating mode all the internal blocks are enabled, and the power consumption is about 100uA.

Over Temperature Protect

IF the WD3151 reaches 135℃, the chip operation is disabled and changed to Standby mode, until temperature drops below 120℃.

I^{2}C Interface

Interface Overview

The I^{2}C interface is built in the WD3151. It can be compatible with 1.8V, 2.8V, 3V and 3.3V. It provides access to the programmable functions and registers on the device.

This protocol uses a two-wire interface for bidirectional communications between the IC's connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL). These lines should be connected to a positive supply, via a pull-up resistor (4.7kΩ) and remain HIGH even when the bus is idle.

Data Transactions

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock’s high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following

sections provide further details of this process.

The Master device on the bus always generates the Start and Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy and it retains this status until a certain time after a Stop Condition is generated. A high-to-low transition of the data line (SDA) while the clock (SCL) is high indicates a Start Condition. A low-to-high transition of the SDA line while the SCL is high indicates a Stop Condition.

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a register read cycle.

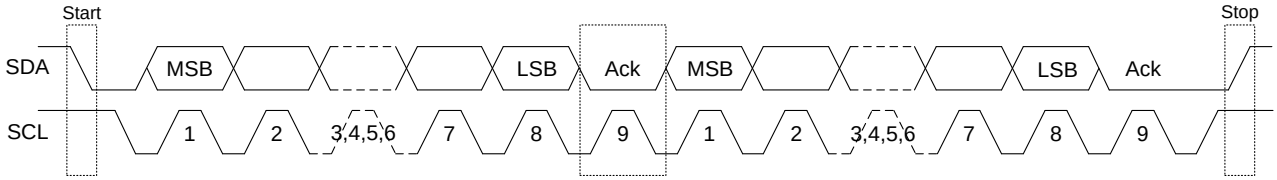


Fig5 I2C data transactions

Addressing Transfer Formats

The WD3151 operates as a slave device with the 7-bit address. If 8-bit address is used for programming, the 8th bit is 1 for read and 0 for write.

Bit7	Bi6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Device address: 45h							R/W

Before any data is transmitted, the master transmits the address of the slave being addressed. The slave device should send an acknowledge signal on the SDA line, once it recognizes its address.

The slave address is the first seven bits after a Start Condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address - the eighth bit.

When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1:read, 0:write), the device acts as a transmitter or a receiver.

The default device address is 45h. The WD3151 allows the user to modify the device address. Through configuration the register IADR (address 77h), the address can be replaced by other values.

Bit7	Bi6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ASEL	Device address: DA<6:0>						

When ASEL = 0, device address =45h (default);

When ASEL = 1, device address = DA<6:0>.

Once the device address is redefined, the master must use the new address. After power-on-reset or soft reset, the device address will be reset to the default value (45h).

Control Register Write Cycle

① Master device generates start condition.
② Master device sends slave address IADR<6:0> and the data direction bit (R/W=0).
③ Slave device sends acknowledge signal if the slave address is correct.
④ Master sends control register address (8bits).
⑤ Slave sends acknowledge signal.
⑥ Master sends data byte to be written to the addressed register (8bits).
⑦ Slave sends acknowledge signal.
⑧ If master will send further data bytes the control register address will be incremented by one after acknowledge signal.
⑨ Write cycle ends when the master creates stop condition.

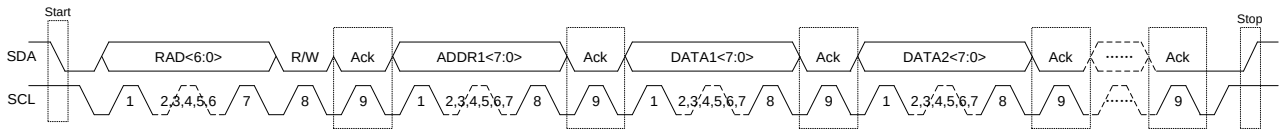
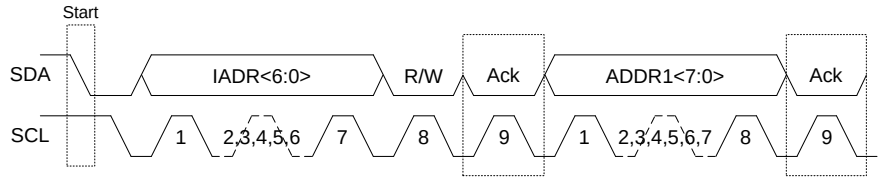
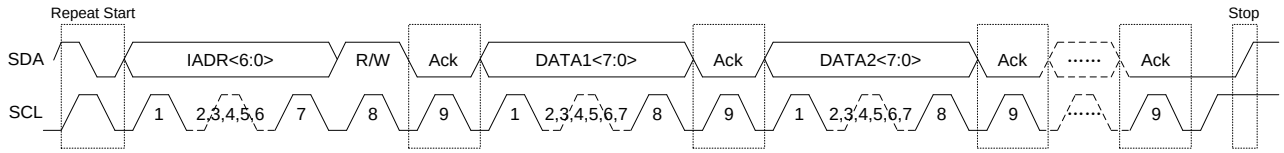


Fig6 I^2C Write Cycle

Control Register Read Cycle

① Master device generates a start condition.
② Master device sends slave address IADR<6:0> and the data direction bit (R/W=0).
③ Slave device sends acknowledge signal if the slave address is correct.
④ Master sends control register address (8 bits).
⑤ Slave sends acknowledge signal.
⑥ Master device generates repeated start condition.
⑦ Master sends the slave address IADR<6:0> and the data direction bit (R/W=1).
⑧ Slave sends acknowledge signal if the slave address is correct. Slave sends data byte from addressed register.
⑨ If the master device sends acknowledge signal, the control register address will be incremented by one. Slave device sends data byte from addressed register.
⑩ Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.





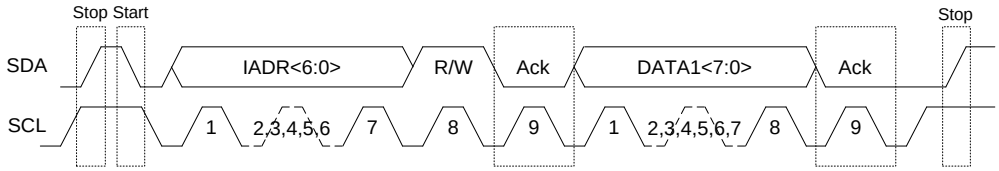


Fig7 I²C Read Cycle

Interrupt

INTN is the interrupt open-drain output pin. It will output low once the programmable lighting sequence running time duration is complete.

The interrupt function is enabled by the high 3-bits of Register GCR.

LED Controller

LED Controller Overview

WD3151 has three independent programmable channels (LED0, LED1, LED2). Trigger connections between channels are common for all channels. All channels have own program memories for storing complex patterns. Brightness control and patterns are done with 8-bit PWM control to get accurate and smooth color control.

Disabled

Each channel can be configured to disabled mode. LED output current will be 0 during this mode.

LED Output Current Setting

LED output current is defined by IMAX bit (Register LCFG0~3).

PWM Setting

Set PWM output value from 0 to 255 by Register PWM0~2.

Direct Control Mode

I²C direct control mode is enabled by the MD bit of Register LCFGx. Changes to the PWM value registers are reflected immediately to the LED brightness.

The WD3151 has fade-in and fade-out function.

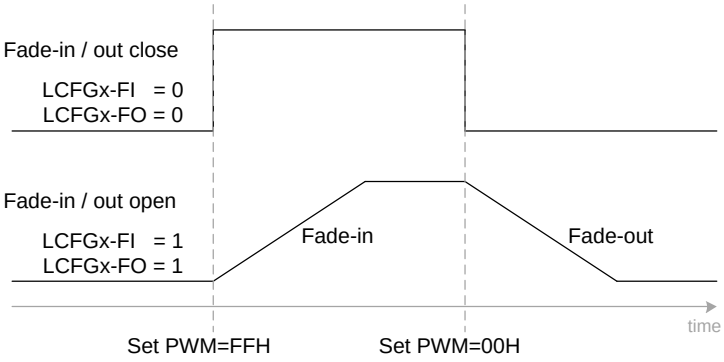


Fig8 Fade-in and Fade-out Function

Program Execution Engines

Use of program execution engines is the other LED output PWM control method available in the WD3151. The device has 3 program execution engines. These engines can be enabled by MD bit of Register LCFGx, and create PWM controlled lighting patterns to the mapped LED outputs according to program codes developed by the user. Program coding is done using programming commands. Programs are loaded into SRAM memory and engine control bits are used to run these programs autonomously. The engines have different operation modes, program execution states, and program counters. Each engine has its own section of the SRAM memory.

The LED pattern is illustrated in the Fig9 below. The cycle is defined with T0~T4 (Fig9). It is possible to program very fast and also very low ramps. The repeat time is defined by REPEAT bits of LEDxT2.

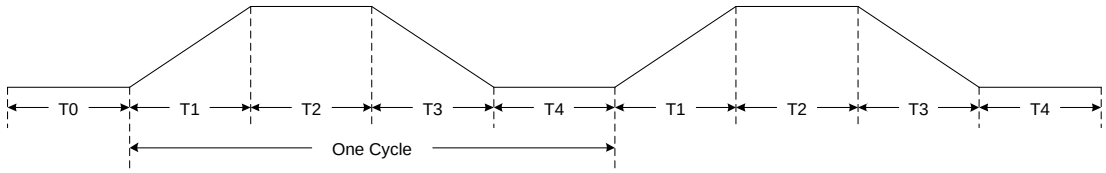


Fig9 LED Lighting Pattern for Program Execution Engines

Register Definition

Register List

Addr (HEX)	Register	Function
00	Reset Register	Reset all registers
01	Operation Enable Register	Chip enable and interrupt enable
02	Interrupt Register	Interrupt status
30	Channel Enable Register	Channel enable
31~33	Lighting Mode Register	LED0~LED2 lighting mode
34~36	PWM Control Register	PWM value of LED0~2
37/3A/3D	T1 & T2 Setting Register	T1 & T2 setting
38/3B/3E	T3 & T4 Setting Register	T3 & T4 setting
39/3C/3F	T0 & Repeat time Setting Register	T0 & repeat time setting
77	Redefined ID Register	Redefined ID

Register Maps

Addr	Register	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	RSTR	WR	0	0	1	1	0	0	1	1
01h	GCR	WR	LIE2	LIE1	LIE0	Reserved				ENABLE
02h	ISR	R	LIS2	LIS1	LIS0	PUIS	Reserved			
30h	LCTR	WR	Reserved					LE2	LE1	LE0
31h	LCFG0	WR	0	FO	FI	MD	0	0	IMAX	
32h	LCFG1	WR	0	FO	FI	MD	0	0	IMAX	
33h	LCFG2	WR	0	FO	FI	MD	0	0	IMAX	
34h	PWM0	WR	PWM							
35h	PWM1	WR	PWM							
36h	PWM2	WR	PWM							
37h	LED0T0	WR	0	T1			0	T2		
38h	LED0T1	WR	0	T3			0	T4		
39h	LED0T2	WR	T0				REPEAT			
3Ah	LED1T0	WR	0	T1			0	T2		
3Bh	LED1T1	WR	0	T3			0	T4		
3Ch	LED1T2	WR	T0				REPEAT			
3Dh	LED2T0	WR	0	T1			0	T2		
3Eh	LED2T1	WR	0	T3			0	T4		
3Fh	LED2T2	WR	T0				REPEAT			
77h	IADR	WR	ASEL	DA[6:0]						

Register Description

Reset Register RSTR

Address: 00h

Default value: 33h

Bit7	Bi6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RST<7>	RST<6>	RST<5>	RST<4>	RST<3>	RST<2>	RST<1>	RST<0>

Description:

Symbol	Bit	Type	Active	Description
RST<7:0>	7:0	WR		Reset all register values when 55h is written.

Operation Enable Register GCR

Address: 01h

Default value: 00h

Bit7	Bi6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LIE2	LIE1	LIE0	Reserved				ENABLE

Description:

Symbol	Bit	Type	Active	Description
LIE2	7	WR	High	LED2 output enable
LIE1	6	WR	High	LED1 output enable
LIE0	5	WR	High	LED0 output enable
Reserved	4:1	WR		
ENABLE	0	WR	High	Chip enable.

Interrupt Register ISR

Address: 02h

Default value: 00h

Bit7	Bi6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LIS2	LIS1	LIS0	PUIS	Reserved			

Description:

Symbol	Bit	Type	Active	Description
LIS2	7	WR	High	LED2 interrupt enable.
LIS1	6	WR	High	LED1 interrupt enable.
LIS0	5	WR	High	LED0 interrupt enable.
PUIS	4	WR	High	Power on reset interrupt.
Reserved	3:0	WR		

Lighting Mode Register LCFG0~2

Address: 31~33h

Default value: 00h

Bit7	Bi6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	FO	FI	MD	0	0	IMAX	

Description:

Symbol	Bit	Type	Active	Description
FO	6	WR	High	Fade-out enable 1: Fade-out time = T3 0: Disable. This function is enabled during Direct Control Mode
FI	5	WR	High	Fade-in enable 1: Fade-in time = T1 0: Disable This function is enabled during Direct Control Mode
MD	4	WR	High	Lighting mode control 0: Direct Control Mode 1: Programmable Lighting Mode
IMAX	1:0	WR		Output current setting 00: 0mA (default) 01: 5mA 10: 10mA 11: 15mA

PWM Control Register PWM0~2

Address: 34~36h

Default value: 00h

Bit7	Bi6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM<7:0>							

Description:

Symbol	Bit	Type	Active	Description
PWM	7:0	WR		Output PWM value setting 0: no PWM 255: 100% duty

T1 & T2 Setting Register LEDiT0

Address: 37h, 3Ah, 3Dh

Default value: 00h

Bit7	Bi6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	T1			0	T2		

Description:

Symbol	Bit	Type	Active	Description
T1	6:4	WR		Fade-in time setting 000: 0.13s 001: 0.26s 010: 0.52s 011: 1.04s 100: 2.08s 101: 4.16s 110: 8.32s 111: 16.64s
T2	2:0	WR		Hold time setting after fade-in 000: 0.13s 001: 0.26s 010: 0.52s 011: 1.04s 100: 2.08s 101: 4.16s Others: 4.16s

T3 & T4 Setting Register LEDiT1

Address: 38h, 3Bh, 3Eh

Default value: 00h

Bit7	Bi6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	T3			0	T4		

Description:

Symbol	Bit	Type	Active	Description
T3	6:4	WR		Fade-out time setting 000: 0.13s 001: 0.26s 010: 0.52s 011: 1.04s 100: 2.08s 101: 4.16s 110: 8.32s 111: 16.64s
T4	2:0	WR		Hold time setting after fade-out 000: 0.13s 001: 0.26s 010: 0.52s 011: 1.04s 100: 2.08s 101: 4.16s 110: 8.32s 111: 16.64s

T0 & Repeat time Setting Register LEDiT2

Address: 39h, 3Ch, 3Fh

Default value: 00h

Bit7	Bi6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T0				REPEAT			

Description:

Symbol	Bit	Type	Active	Description
T0	7:4	WR		Delay time setting before auto blinking 000: 0s 001: 0.13s 010: 0.26s 011: 0.52s 100: 1.04s 101: 2.08s 110: 4.16s 111: 8.32s 1000: 16.64s Others: 16.64s
REPEAT	3:0	WR		Blinking times setting 0000: Continuous blinking 0001: 1 time 0010: 2 times …… 1111: 15 times

Redefined ID Register IADR

Address: 77h

Default value: 45h

Bit7	Bi6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ASEL	DA<6:0>						

Description:

Symbol	Bit	Type	Active	Description
ASEL	7	WR	High	ID select: 0: ID 45h (default) 1: ID DA[6:0]
DA<6:0>	6:0	WR		Redefined ID only if ASEL=1

Package outline dimensions

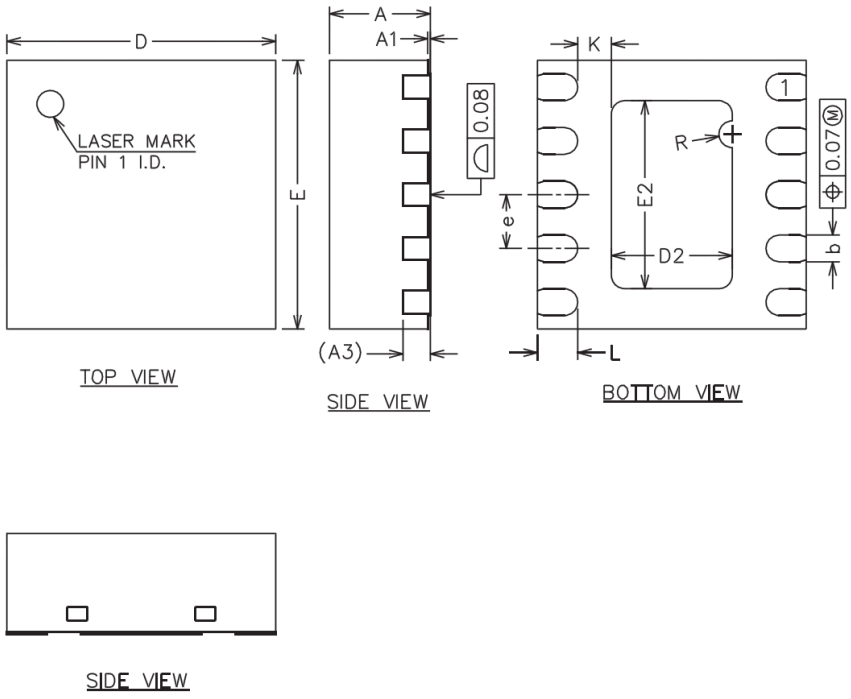


Fig10 DFN2*2-10L Outline Dimensions

Symbol	Dimensions in millimeter		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.15	0.20	0.25
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.80	0.90	1.00
E2	1.30	1.40	1.50
e	0.30	0.40	0.50
K	0.15	0.25	0.35
L	0.25	0.30	0.35
R		0.10REF	